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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
KNOLL, CLIFFORD H	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 05/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,938	APOSTOL ET AL.	
	Examiner	Art Unit	
	Clifford H. Knoll	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,11-35,39 and 40* is/are rejected.

7)☒ Claim(s) *36-38* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date Sdlnt. 2/6/06
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is responsive to communication filed 8/22/05. Currently claims 1-9 and 11-40 are pending; claim 10 has been cancelled.

Claim Rejections - 35 USC § 103

1. *Claims 1-4, 6-9, 11-20, 22-29, 31-35, and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen (US 5197130) in view of Grace (US 6560160 B1).*

Regarding claims 1, 16, and 17, Chen discloses an array of memory cells (e.g., col. 14, lines 30-39); a first data transfer interface coupled to the array of memory cells to provide a first access path for a selected one of a processor and a plurality of subsystems of the IC to access said array of memory cells (e.g., Figure 10; col. 17, lines 48-51) a second data transfer interface coupled to the array of memory cells to provide a second access path for said processor to access said array of memory cells (e.g., col. 20, lines 53-54; Figure 10, "Section 8: "50"); and a controller coupled to the array of memory cells and the first and second data transfer interfaces to control said array of memory cells and said first and second data transfer interfaces to facilitate concurrent accesses of said memory unit by said processor and said subsystems (e.g., Fig. 19a, "44"). Chen also discloses the second access path provides access to the memory cell accessible through the first access path (e.g., Fig. 17, "Bank Decoders" which arbitrate for access among all interfaces, col. 20, lines 15-16).

Chen does not expressly mention that the second data transfer interface having priority over the first data transfer interface; however Grace discloses this (col. 4, lines 31-37). It would have been obvious to one of ordinary skill in the art to combine Grace with Chen because Grace teaches the advantages of using sequenced access in a multiport memory (e.g., col. 1, lines 47-55).

Regarding claims 2 and 18, Chen also discloses the first data transfer interface comprises a first inbound queue coupled to said array of memory cells for queuing a first plurality of memory accesses of said processor and said subsystem of a first priority; a second inbound queue coupled to said array of memory cells for queuing a second plurality of memory accesses of said processor and said subsystem of a second priority (e.g., Fig. 14, "324"); and an outbound queue coupled to said array of memory cells for queuing output responses to said first and second plurality of memory accesses of said processor and said subsystem of said first and second priorities accessed through said first and second inbound queues (e.g., Fig. 14, "326").

Regarding claims 3 and 19, Chen also discloses second data transfer interface comprises an inbound queue coupled to said array of memory cells for queuing a first plurality of memory accesses of said processor; and an outbound queue coupled to said array of memory cells for queuing output responses to said first plurality of memory accesses of said processor (e.g., col. 17, lines 48-51).

Regarding claims 4 and 20, Chen also discloses controller comprises a sequential storage structure coupled to said array of memory cells (e.g., Fig. 14, "330"); a multiplexor (e.g., Fig. 14, "320", Fig. 13, "44"), coupled to inbound queues of said first

and second data transfer units and said sequential storage structure to sequence memory accesses queued in said inbound queues into said sequential storage structure; and a state machine coupled to said sequential storage structure, said multiplexor, and said inbound queues of said first and second data transfer units to control their operation (e.g., Fig. 14, "332").

Regarding claims 6 and 22, Chen also discloses sequence memory accesses queued in inbound queues of said first data transfer interface into said sequential storage structure, in accordance with assigned priorities of said inbound queues (e.g., col. 17, lines 59-64).

Regarding claims 7 and 23, Chen also discloses the controller comprises a first sequential storage structure to stage headers for output responses to memory accesses (e.g., col. 22, lines 27-29); a second sequential storage structure coupled to said array of memory cells to stage output responses to memory accesses (e.g., Fig. 14, "334"); a first multiplexor coupled to said first and second sequential storage structures to selective output one of said staged headers of output responses to memory accesses and said staged output responses to memory accesses (e.g., col. 22, lines 30-32); a second multiplexor coupled to said first multiplexor and outbound queues of said first and second data transfer units to selective output the selected output of said first multiplexor to a selected one of said outbound queues of said first and second data transfer unit (e.g., Fig. 14, "SECTION PATH", "326"); and a state machine coupled to said first and second sequential storage structures, said first and second multiplexors,

and said outbound queues of said first and second data transfer units to control their operation (e.g., Fig. 14, "332").

Regarding claim 8, Chen discloses queuing first memory accesses of a processor and a plurality of subsystems of the IC in inbound queues of a first data transfer interface (e.g., col. 20, lines 53-54); queuing second memory accesses of the processor in an inbound queue of a second data transfer interface (e.g., Fig. 14, "324"); sequencing said first and second memory accesses into a single sequence of memory accesses (e.g., Fig. 14, "332"; col. 17, lines 48-51); and servicing said first and second memory accesses in accordance with their sequence order (e.g., col. 17, lines 36-40).

Chen does not expressly mention that the second memory access is sequenced before any first memory access; however Grace discloses this (col. 4, lines 31-37). It would have been obvious to one of ordinary skill in the art to combine Grace with Chen because Grace teaches the advantages of using sequenced access in a multiport memory (e.g., col. 1, lines 47-55).

Regarding claim 9, Chen also discloses where queuing of said first memory accesses in inbound queues of a first data transfer interface comprises queuing said first memory accesses into inbound queues of said first data transfer interface having associated priorities, in accordance with priorities of said first memory accesses (e.g., col. 18, lines 41-44).

Regarding claim 11, Chen also discloses wherein said sequencing comprises sequencing first memory accesses queued in inbound queues of said first data transfer

interface, in accordance with assigned priorities of the inbound queues (e.g., col. 17, lines 59-64).

Regarding claim 12, Chen also discloses wherein said servicing comprises generating and queuing headers for output responses to said first and second memory accesses (e.g., col. 17, lines 48-51).

Regarding claim 13, Chen also discloses said servicing comprises queuing output responses to said first and second memory accesses (e.g., Fig. 14, "SECTION PATH", "326").

Regarding claim 14, Chen also discloses merging headers for output responses to said first and second memory accesses and output responses to said first and second memory accesses (e.g., col. 22, lines 30-32).

Regarding claim 15, Chen also discloses selectively outputting headers for output responses to said first and second memory accesses and output responses to said first and second memory accesses to a selected one of said first and said second data transfer interfaces (e.g., col. 22, lines 30-32).

Regarding claim 24, Chen also discloses an on-chip bus (e.g., col. 14, lines 40-42).

Regarding claim 25, Chen also discloses a data traffic router to which said memory unit, said processor, and at least one of said subsystems is attached, said data traffic router facilitating concurrent communication between selected combinations of said memory unit, said processor and said at least one subsystem (e.g., col. 16, lines 41-44).

Regarding claim 26, Chen also discloses a collection of peripheral device controllers (e.g., col. 10, lines 56-66).

Regarding claim 27, Chen discloses making first memory accesses of a memory unit of the IC via a first access path in turn; the processor also successively making second memory accesses to said memory unit via a second access path in parallel (e.g., col. 15, lines 52-59); and the memory unit servicing said first and second memory accesses made through said first and second access paths in parallel (e.g., col. 22, lines 26-27, the memory unit of Chen is provided as parallel units).

Chen does not expressly mention that the second memory access is sequenced before any first memory access; however Grace discloses this (col. 4, lines 31-37). It would have been obvious to one of ordinary skill in the art to combine Grace with Chen because Grace teaches the advantages of using sequenced access in a multiport memory (e.g., col. 1, lines 47-55).

Regarding claim 28, Chen also discloses queuing said first memory accesses of said processor and said plurality of subsystems of the IC in inbound queues of a first data transfer interface of said memory unit; queuing said second memory accesses of the processor in an inbound queue of a second data transfer interface of said memory unit (e.g., col. 20, lines 53-54); sequencing said first and second memory accesses into a single sequence of memory accesses (e.g., Fig. 14, "320", Fig. 13, "44"); and servicing said first and second memory accesses in accordance with their sequence order (e.g., col. 18, lines 41-44).

Regarding claim 29, Chen also discloses queuing of said first memory accesses of said processor and said plurality of subsystems of the IC in inbound queues of a first data transfer interface comprises queuing said first memory accesses into inbound queues of said first data transfer interface having associated priorities, in accordance with priorities of said first memory accesses (e.g., col. 17, lines 59-64).

Regarding claim 31, Chen also discloses sequencing first memory accesses queued in inbound queues of said first data transfer interface, in accordance with assigned priorities of the inbound queues (e.g., col. 17, lines 59-64).

Regarding claim 32, Chen also discloses generating and queuing headers for output responses to said first and second memory accesses (e.g., col. 17, lines 48-51).

Regarding claim 33, Chen also discloses queuing output responses to said first and second memory accesses (e.g., Fig. 14, "SECTION PATH", "326").

Regarding claim 34, Chen also discloses merging headers for output responses to said first and second memory accesses and output responses to said first and second memory accesses (e.g., col. 22, lines 30-32).

Regarding claim 35, Chen also discloses selectively outputting headers for output responses to said first and second memory accesses and output responses to said first and second memory accesses to a selected one of said first and said second data transfer interfaces (e.g., col. 22, lines 30-32).

Regarding claim 39, Chen also discloses the multiplexor for sequencing memory accesses (e.g., Fig. 17, "Bank 0 Inhibit Matrix" et al., col. 20, lines 16-22).

2. *Claims 5, 21, and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Chen as applied in parent claims supra, in view of Agarwala (US 6681270).*

Regarding claims 5, 21, and 30, Chen discloses prioritizing transfers, but does not expressly mention sequencing accesses in the second transfer interface before sequencing the accesses in the first data transfer interface; however this detail is disclosed by Agarwala. Agarwala discloses setting fixed priorities for transfer units (e.g., col. 3, lines 44-45). It would have been obvious to combine Agarwala with Chen, because Agarwala teaches the advantages of the standard practice in which a data transfer interface ("channel") is assigned a particular priority. Therefore, it would have been obvious to one of ordinary skill in the art to combine Agarwala with Chen to obtain the claimed invention.

3. *Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen and Grace, in view of Mulla (US 6557078 B1).*

Regarding claim 40, Chen, applied in parent claim 1, also discloses dedicated memory accesses from the processor (e.g., Fig. 5, "114", col. 11, lines 45-49). Chen does not expressly admit the configuration of dedicated access to the second transfer controller (having gone through preceding arbitration at e.g., Fig. 14, "320"); however, dedicating a port in memory to a particular data type is well known, as seen in Mulla, who teaches dedicated data queuing in a multiport system (e.g., col. 7, lines 37-40). It would have been obvious to combine Mulla with Chen because Mulla's dedicated cache allows higher performance (e.g., col. 3, lines 60-67; col. 4, lines 4-6).

Allowable Subject Matter

4. Claims 36-38 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the interactions claimed between the processor and the subsystem distinguish them from the prior art.

Response to Arguments

Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H. Knoll whose telephone number is 571-272-3636. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rehana Perveen can be reached on 571-272-3676. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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